Abstract

A semiconductor device structure, includes a PMOS device **200** and an NMOS device **300** disposed on a substrate **1,2**, the PMOS device including a compressive layer **6** stressing an active region of the PMOS device, the NMOS device including a tensile layer **9** stressing an active region of the NMOS device, wherein the compressive layer includes a first dielectric material, the tensile layer includes a second dielectric material, and the PMOS and NMOS devices are FinFET devices **200, 300.**

(Fig. 17)